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Customer No.: 31561
Docket No.: 11584-US-PA
Application No.: 10/708,446

AMENDMENT

Please amend the application as indicated hereafter.

To the Specification:

Please disregard the amendments addressed to paragraphs [0002], [0003], [0005] and [0026] submitted on Dec. 11, 2006 and amend the paragraphs as followed.

Please amend paragraph [0005] as follows:

[0005] The driving circuit for a liquid crystal display (LCD) in conventional scheme is primarily categorized into a parallel driving circuit and a cascade driving circuit. A parallel driving circuit transmits a data signal to designated a driving circuit unit via a bus, thus it takes a substantially large layout and routing area on a printed circuit board.

Please amend paragraph [0006] as follows:

[0006] Referring FIG. 1, a parallel driving circuit structure is illustrated herein. The data signal 122 of the LCD 110 in the figure is supplied by a plurality of driving circuit units 120, which are manufactured with Tape Carrier Package (TCP) technology. The driving circuit units 120 supplies primitive data signal 144 via data bus 142, and the data signal 144 is transmitted to designated driving circuit unit 120 via data bus 142 controlled by a timing controller 140. The foregoing data bus 142 and the timing controller 140 are both disposed on a printed circuit board 130. Since bus structure and timing controller are included, significant layout and routing area on the printed circuit board 130 are required. Therefore, a cascade style driving circuit [[is]]was developed [[upon]]for pursuing ~~miniature~~ miniaturization in electronic products.

Please amend paragraph [0008] as follows:

[0008] Referring to FIG. 2, a cascade driving circuit structure is described herein. The data signal 222 for the LCD 210 in the figure is supplied by a plurality of driving circuit units 220, which is formed via Chip On Glass (COG) technology on LCD substrate 210. The timing controller 240, being disposed on the PCB 230, generates cascade signal 224 and transmits ~~which~~ the cascade signal to a designated driving unit 220 stage by stage via the cascade structure of the driving circuit units 220. The transmitting channel of the cascade signal 224 is formed on the LCD substrate 210 with Wire On Array (WOA) technology.

Please amend paragraph [0029] as follows:

[0029] The aforementioned differential signal transmitter 430 and the receiver 420 are illustrated as shown in FIG. 5. In the figure, the drains of the transistor 520 and transistor 530 are coupled to the current source 510, the source of the transistor 520 is coupled to the drain of the transistor [[520]]540 where an output signal 522 is drawn, the source of the transistor 530 is coupled to the drain of the transistor 550 where output signal 532 is drawn, and the sources of the transistor 540 and of the transistor 550 are coupled to ground voltage. The signal 522 and the signal 532 make the differential signal that is transmitted by the differential transmitter 501. The differential signal receiver 502 couples the signal 522 to a first end of the resistor 570 and the negative terminal of the amplifier 560, and couples the signal 532 to a second end of the resistor 570 and the positive terminal of the amplifier 560.